

Amendments to the Claims:

Claims 1-145 Cancelled.

146. (New) A design verification method, in which one or more design bugs in a design code or in a design net-list are identified by simulation with one or more test benches, comprising the following steps: at least one simulation execution with a test bench consisting of a 1st simulation run as a front-stage simulation and one or more post-1st simulation runs as a back-stage simulation, wherein a necessary information is collected from the 1st simulation run when the 1st simulation run is in progress, and said one or more post-1st simulation runs are executed by using said collected necessary information for obtaining visibility.

147. (New) A design verification method, in which one or more design bugs in a design code or in a design net-list are identified by simulation with one or more test benches, comprising the following steps: at least one simulation execution with a test bench consisting of a 1st simulation run as a front-stage simulation and one or more post-1st simulation runs as a back-stage simulation, wherein a necessary information is collected from the 1st simulation run when the 1st simulation run is in progress, and said one or more post-1st simulation runs are executed by using said collected necessary information for obtaining visibility, and said necessary information consists of the values on all inputs and input/outs signals in one or more design objects and the design state of said one or more design objects.

148. (New) A design verification method, in which one or more design bugs in a design code or in a design net-list are identified by simulation with one or more test benches, comprising the following steps: at least one simulation execution with a test bench consisting of a 1st simulation run as a front-stage simulation and one or more post-1st simulation runs as a back-stage simulation, wherein a necessary information is collected from a 1st simulation run when a 1st simulation run is in progress, said one or more post-1st simulation runs are executed by using said collected necessary information for obtaining visibility, the values on all inputs and input/outs signals in one or more design objects are saved for the entire simulation time of said 1st simulation run for said necessary information collected from said 1st simulation run, one or more design states of said one or more design objects are also saved only at

regular intervals in said 1st simulation run for said necessary information collected from said 1st simulation run, and said one or more post-1st simulation runs are executed only for the partial simulation time in said entire simulation time of said 1st simulation run.

149. (New) A design verification method, in which a simulation run at a lower level of abstraction is executed by using simulation results collected from one or more simulation runs at a higher level of abstraction.

150. (New) A design verification method according to Claim 149 wherein:

said simulation results collected from one or more simulation runs at the higher level of abstraction, which is used at a simulation run at the lower level of abstraction, contain one or more design states of the design at the higher level of abstraction, and said simulation run at the lower level of abstraction is executed in temporally parallel.

151. (New) A design verification method comprising: by using a verification software and at least one or more verification platforms an additional code or circuit is instrumented into a design code or into a design net-list in an automatic way so that dynamic information is collected by said additional code or circuit instrumented during one or more verification runs (simulation runs or simulation acceleration runs), and the collected dynamic information is re-used at a post-debugging simulation after at least one design object is changed for debugging for reducing a total verification time.

152. (New) A design verification method according to Claim 151, wherein for said collected dynamic information the values on all inputs and outputs signals in one or more design objects are saved during said one or more verification runs (simulation runs or simulation acceleration runs), and one or more design states of one or more design objects are also saved only at regular intervals during said one or more verification runs (simulation runs or simulation acceleration runs), and

after at least one design object is changed for debugging said post-debugging simulation includes the following two simulation steps;

- i) first, only said simulation input stimuli (input information for replay), and the values on its outputs are compared with that of the design object saved during said one or

more verification runs (simulation runs or simulation acceleration runs) before at least one design object is changed for debugging, and during this simulation one or more design states of said design object changed for debugging are also saved only at said regular intervals, and this simulation stops when the values on its outputs are different from that of the design object saved during said one or more verification runs(simulation runs or simulation acceleration runs) before at least one design object is changed for debugging,

ii) second, both changed design object and unchanged design objects are simulated together, but, unchanged design objects are simulated not from the simulation time 0, but from one of the design checkpoints made in said one or more verification runs(simulation runs or simulation acceleration runs) after restoring the design state for said unchanged design object, which had been previously saved during said one or more verification runs(simulation runs or simulation acceleration runs).